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FOR

ELECTROSTATIC DISCHARGE PROTECTION DEVICE AND METHOD THEREFOR

Inventor(s): Lawrence T. Clark
Pradeep Elamachili
Timothy J. Maloney

Prepared by: Kenneth M. Seddon,
Patent Attorney

intel®
Intel Corporation
5000 W. Chandler Blvd., CH6-404
Chandler, AZ 85226-3699
Phone: (480) 554-9732
Facsimile: (480) 554-7738

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ELECTROSTATIC DISCHARGE PROTECTION DEVICE AND METHOD THEREFOR

BACKGROUND

One technique to protect the components (e.g., transistors, inactive devices, etc) of an integrated circuit from an electrostatic discharge (ESD) event is to add circuitry intended to sink or remove the charge associated with the ESD event. For example, a wide clamping device (e.g. a transistor having a width significant to allow the charge to drain away without creating a damaging current density) may be placed in parallel or in series with the portion of the integrated circuit to be protected. Due to the width of the clamping device, it is typically able to sink the charge associated with the ESD device and alleviate high voltage levels that may otherwise result.

However, as manufacturing techniques improve, the channel length of transistors is typically reduced, which, in turn, may increase the sub-threshold leakage of the transistors. Consequently, the clamping devices may become a significant source of leakage current while the integrated circuit is in operation. Thus, there is a continuing need for better ways to provide charge protection to an integrated that have reduced leakage currents.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects,

features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a schematic representation of a portion of an integrated circuit having a charge protection device in accordance with an embodiment of the present invention;

FIG. 2 is a cross-sectional and top view of a portion of a charge protection device in accordance with an embodiment of the present invention; and

FIGs. 3-4 are schematic representations of alternative embodiments of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to

obscure the present invention.

In the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

Turning to FIG. 1, an embodiment 100 in accordance with the present invention is described. Embodiment 100 may comprise a portable device such as a mobile communication device (e.g., cell phone), a two-way radio communication system, a one-way pager, a two-way pager, a personal communication system (PCS), a portable computer, or the like. Although it should be understood that the scope and application of the present invention is in no way limited to these examples.

Embodiment 100 here includes an integrated circuit 10 that may comprise, for example, a microprocessor, a digital signal processor, a microcontroller, or the like. However, it should be understood that only a portion of integrated circuit 10 is included in FIG. 1 and that the scope of the present invention is not limited to these examples. Integrated circuit 10 may comprise core logic 20 that may include transistors that are perform the instructions or operations executed by integrated circuit 10.

Although the scope of the present invention is not limited in this respect,

integrated circuit 10 may be coupled to a power supply voltage potential, labeled Vcc in FIG. 1. For example, Vcc may range from about 0.5-2.5 volts above ground. As shown in FIG. 1, the power supply voltage potential may be provided from an external pin upon which an electrostatic discharge event may occur. An electrostatic discharge event may be caused by a variety of situations depending upon the environment in which integrated circuit 10 is placed. Simply stated, although the scope of the present invention is not limited in this respect, an electrostatic discharge (ESD) event may occur when excess charge is present on the pin used to provide the power supply voltage potential. This may occur if integrated circuit 10 comes in electrical contact with something having excess charge (e.g., physical contact by a human being or a piece of manufacturing equipment).

To reduce the likelihood that the excessive charge may damage the active or inactive components of core logic 20, integrated circuit 10 may comprise a charge protection device that is used to provide a low impedance path that provides a path for the excessive charge to ground. For example, integrated circuit 10 may comprise a p-channel Metal-oxide Semiconductor (PMOS) device 50 that is capable of sinking the excess charge associated with an ESD event.

Although the scope of the present invention is not limited in this respect, transistor 50 may be manufactured so that it provides a path for the excessive charge to ground that is of lower impedance than the transistors and components of core logic 20. The physical dimensions of transistor 50 may vary depending on

the manufacturing technology used and the electrical characteristics of the transistors in core logic 20. For example, transistor 50 may have a width of at least 500 microns and a channel length of less than about 0.2 microns, although the scope of the present invention is not limited in this respect. It should be understood the physical and electrical characteristics of transistor 50 may be altered so that transistor 50 is capable of carrying a desired amount of pulsed current. In this particular embodiment, transistor 50 may be able to conduct at least 1 amp or more depending on factors such as its width. In alternative embodiments, transistor 50 may be capable of conducting a pulsed 5-10 amps without any adverse effects.

Integrated circuit 10 may optionally comprise a PMOS transistor 32, a capacitor 40, and a resistive element 55 that may be used to enable the charge protection device during an ESD device. Excess charge on the power supply voltage potential source, Vcc, may cause transistor 32 to conduct, which, in turn will place a voltage potential on capacitor 40.

Integrated circuit 10 may also optionally comprise timer or delay units that may be used to enable the operation of clamping transistor 50 and a biasing transistor 31. For example, transistors 35-36 may act as an inverter that enables biasing transistor 31 if there is a voltage potential stored on capacitor 40 (e.g., during an ESD event). Transistors 33-34 and 37-38 may act as two inverters in series that enable the operation of clamping transistor 50. However, clamping transistor 50 may be substantially enabled after biasing transistor 31 due to the

extra inverter in the path of the enabling signal. As explained in more detail below, biasing transistor 31 may be desirable so to offset or compensate the reverse biasing of clamping transistor 50 that may occur while integrated in under normal operation (e.g. integrated circuit if performing its intended operations such as executing instructions, storing data, processing data, etc.). This may allow transistor 50 to conduct more current during an ESD event.

Integrated circuit 10 may also comprise a resistive element 30 that may be used to reverse bias the charge protection device, clamping transistor 50. As shown in FIG. 1, resistive element 30 may be a n-channel Metal-oxide Semiconductor (NMOS) transistor whose gate terminal and drain region are coupled to a voltage potential, labeled Vccp. Although the scope of the present invention is not limited in this respect, Vccp may be higher or greater than the power supply voltage potential, Vcc. As should be apparent, in the embodiment shown in FIG. 1, transistor 30 is in a source follower arrangement, although, again, the scope of the present invention is not limited in this respect.

While integrated circuit 10 is in normal operation (e.g. embodiment 100 is in use and/or there is no ESD event), resistive element 30 may provide a voltage potential (e.g. approximately Vccp) to the bulk region of clamping transistor 50. This, in turn, may reverse bias clamping transistor 50 since the source region of clamping transistor 50 is at a lower voltage potential (e.g., Vcc). If the charge protection device (e.g. clamping transistor 50) is an enhancement-mode PMOS device, the bulk region may refer to the portion of the semiconductor substrate in

which a conductive channel is formed when a low voltage potential (e.g., 0 volts or ground) is applied to the gate terminal. By applying a voltage potential to the bulk region of transistor 50 that is higher than the voltage potential on the source region of transistor 50, the transistor may be reverse body biased so that the leakage current through transistor 50 when it is in a non-conducting or disabled state is reduced. This, in turn, may reduce the overall power consumption of integrated circuit 10.

When integrated circuit experiences an ESD event (e.g. excess charge is present on the power supply voltage potential line, capacitor 40 and the inverter provided by transistors 35-36 may enable biasing transistor. For example, the excessive charge may, at least in part, result in a high voltage potential on the gate terminal of biasing transistor 31. This, in turn, may cause biasing transistor 31 to conduct so that the power supply voltage potential, Vcc, may be applied to the bulk region of clamping transistor 50. This may be desirable to offset or compensate for the reverse biasing effect provided by resistive element 30 so that clamping transistor 50 may have a lower threshold voltage. Consequently, the charge protection device may provide a path to ground for the excessive charge that has lower impedance than the devices in core logic 50. Consequently, the charge may be dissipated without causing any damage to core logic 50.

It should be understood that resistive element 30 need not be a NMOS transistor in order to reverse bias the charge protection device. In alternative embodiments, resistive element may comprise two or more transistors in series.

Likewise, resistive element 30 may comprise a thick-gate transistor that has a gate oxide that is thicker than the components or transistors of core logic 20, or comprise a diffused or polysilicon resistor. Simply speaking, it may be desirable for resistive element 30 to have an impedance value greater than transistor 31 to reduce the effects of reverse biasing, although the scope of the present invention is not limited in this respect.

FIG. 2 is provided to illustrate an example of for the dense arrangement of biasing transistor 31, although the scope of the present invention is not limited to this particular example. It should be understood that in alternative embodiments, the transistors shown in the figures may have opposite polarity (e.g., n-channel devices instead of p-channel devices, etc.) and the scope of the present invention in not limited to a particular substrate material as alternatives such as semiconductor-on-insulator (SOI) may also be used.

FIG. 2 illustrates a cross-sectional view of biasing transistor along with a corresponding top view of the layout structure. Biasing transistor 31 may be formed in a p substrate 210 and include a gate structure 215 that partially overlaps both p substrate 210 and an n-well region 200. Optionally, the charge protection device, such as clamping transistor 50 may also be formed in n-well region 200 to reduce the amount of interconnect use to couple biasing transistor 31 to clamping transistor 50. This arrangement may protect the gate of transistor 21 from the substantially higher voltage potential on its drain node.

Turning to FIG. 3, an alterative embodiment 300 of a charge protection

device for core logic 20 is provided. In this particular embodiment, more than one transistor may be used to provide the low impedance path to ground for excessive charge on the power supply voltage potential, Vcc. For example, transistors 350-351 are in series and may provide a path to excessive charge so that the components and transistors of core logic 20 are not damaged during an ESD event.

During an ESD event, the excessive charge on the power supply voltage line may cause transistor 315 to conduct so that a logic "0" is stored on capacitor 316. This may indicate that an ESD event is occurring. Transistors 310-312 may provide two inverters in series which may have the effect of enabling transistors 350-351 so that a low impedance path to ground may be provided. As indicated in FIG. 3, the source region of transistor 351 and the bulk region of transistors 350-351 are connected to the power supply voltage potential, Vcc. However, the source terminal of transistor 350 is not connected to Vcc, but rather the drain of transistor 351. Consequently, when the transistors of core logic 20 are in operation, and there is no ESD event, transistors 350-351 are disabled. The source voltage potential of transistor 350 may be at a lower voltage potential than the bulk region of transistor 350. This, in turn, may cause transistor 350 to be reverse body biased.

Reverse body bias on one of the transistors of the charge protection device (e.g., transistor 350) may reduce the leakage current through transistor 350 may be reduced. Since transistor 351 is in series with transistor 350, the leakage current through transistor 351 may be reduced the same or similar amount. Having

multiple transistors in series to provide the charge protection device may be desirable because the combination of transistors in series may allow the charge protection device to protect for ESD events on nodes with higher voltage potentials (e.g., input/output voltages).

As discussed with reference to FIG. 3, it may be desirable to provide a charge protection device by placing two or more clamping transistors in series between the power supply voltage potential (e.g., Vcc and ground). As indicated in FIG. 3, the gate terminal of transistors are enabled by the same signal or voltage potential. Referring now to FIG. 4, in some alternative embodiments, it may be desirable for the transistors that provide the charge protection device to have different threshold voltages or to be enabled by different signals or voltage potentials.

As shown in FIG. 4, a plurality of transistors 410 may be used to provide a voltage divider 411. Voltage divider 411 may be used to provide an output voltage potential that is a fraction of the power supply voltage potential, Vcc. The output voltage potential may be provided to a voltage buffer 430. Voltage buffer 430 may be provided with transistors 420-421 and may be used to amplify or drive a voltage potential to the gate terminal of clamping transistor 450. This particular embodiment may also comprise inverters 460-464 that may be use to delay or time when clamping transistors 450-451 are enabled so that they may provide a low impedance path for excessive charge during an ESD event. As shown in FIG. 4, the source terminal of transistor 450 may float while the bulk region of transistor

450 is connected to the power supply voltage potential. Consequently, transistor 450 may be reverse body biased when there is no ESD event. It should be understood that it may be desirable, in alternative embodiments, to remove transistor 32, resistor 55, and capacitor 40 in an effort to reduce the size of the overall circuit.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

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